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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,226	12/10/2003	William M. Hiatt	108298744US	8010

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EXAMINER	
MATTHEWS, COLLEEN ANN	
ART UNIT	**PAPER NUMBER**
2811	

MAIL DATE	DELIVERY MODE
10/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/733,226	HIATT ET AL.	
	Examiner	Art Unit	
	Colleen A. Matthews	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 28-52* is/are pending in the application.

4a) Of the above claim(s) *12-14 and 37* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,28-36, 38-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE GURLEY
SUPERVISORY PATENT EXAMINER
AU 2811, TC 2800

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

In view of the Appeal Brief filed on 07/09/2007, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 9-10, 28-29, 33, 36, 38-45 and 48-52 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Pat. No. 6,809,421 to Hayasaka et al. (Hayasaka).

Regarding claim 1: Hayasaka discloses a method of forming a conductive interconnect in a microelectronic device (examples in Figures 7A-7I, 8-9, 13A-13C,14A-14D,17A-17B, 33, and 34A-34C), the method comprising:

providing a microfeature workpiece (Fig 33 element 152) having a plurality of dies (Fig 33 element 151_2, 151_3);

forming a passage (Fig 14A, element 13) extending through the microfeature workpiece from a first side of the microfeature workpiece to an opposite second side of the microfeature workpiece (col 16 lines 42-45);

forming a conductive plug (Fig 7D element 15; Fig 13B element 29; Fig 17A element 15; Figs 33,34A-34C element 104) in the passage adjacent to the first side of the microelectronic workpiece; and

depositing conductive material (Fig 13C element 30; Fig 17B element 8; Figs 33, 34A-34C element 156) in the passage to at least generally fill the passage from the conductive plug to the second side of the microelectronic workpiece.

Regarding claim 9: Hayasaka discloses the method of claim 1, further comprising applying a passivation layer (Fig 7C,14,17B element 14) to at least a portion of the passage before forming the conductive plug in the passage and filling the passage from the conductive plug to the second side of the microelectronic workpiece (Fig 17B).

Regarding claim 10: Hayasaka discloses the method of claim 1, further comprising forming a bond-pad (Fig 14D element 17) on the microelectronic workpiece in contact with the conductive plug.

Regarding claim 48: Hayasaka discloses the method of claim 1, further comprising applying a passivation layer (Fig 7C,14,17B element 14) to at least a portion of the passage (Fig 14A, element 13) before forming the conductive plug (Fig 7D element 15; Fig 13B element 29; Fig 17A element 15; Figs 33,34A-34C element 104) in the passage, and wherein depositing conductive material (Fig 13C element 30; Fig 17B element 8; Figs 33, 34A-34C element 156) in the passage to at least generally fill the passage includes depositing the conductive material in contact with the conductive plug and the passivation layer (see Fig 13C, 17B).

Regarding claim 28: Hayasaka discloses a packaged microelectronic device (examples in Figures 13C, 14D, and 17B) comprising:

a die (10/11) having a first side and a second side opposite to the first side, the die further having an integrated circuit positioned between the first and second sides (see circuit within element 11 shown in Figure 9);

a bond-pad (Figure 14D element 17) positioned on the first side of the die and electrically coupled to the integrated circuit;

a passage (Fig 14D, element 13) extending completely through the die (col 16 lines 42-45) and aligned with the bond-pad;

a first conductive material (Fig 13C element 29; Fig 14D, element 15; Fig 17B element 15) deposited in a first portion of the passage adjacent to the first side of the die to form a conductive plug electrically connected to the bond-pad; and

a second conductive material (Fig 13C element 30; Fig 17B element 8) deposited in a second portion of the passage in contact with the conductive plug to at least generally fill the passage from the conductive plug to the second side of the die.

Regarding claim 29: Hayasaka discloses the packaged microelectronic device of claim 28, further comprising an insulative layer (Fig 13C, 17B element 14; Fig 14D element 31) deposited in the passage between the die (10/11) and the first and second conductive materials (Fig 13C elements 29/30; Fig 14D, element 15; Fig 17B elements 15/8).

Regarding claim 49: Hayasaka discloses the packaged microelectronic device of claim 28, further comprising an insulative layer (Fig 13C, 17B element 14; Fig 14D element 31) deposited in the passage, wherein the second conductive material contacts the conductive plug and the insulative layer (see Fig 13C, 17B).

Regarding claim 33: Hayasaka discloses a microfeature workpiece (examples in Figures 13C, 14D, 17B, and 33) having a first side and a second side opposite to the first side, the microfeature workpiece comprising:

at least one die (Fig 33 element 151_2, 151_3);

a passage (Fig 14A, element 13) extending completely through the die from the first side of the microfeature workpiece to the second side of the microfeature workpiece (col 16 lines 42-45);

a first conductive material (Fig 13C element 29; Fig 14D, element 15; Fig 17B element 15; Figs 33 element 104) deposited in a first portion of the passage adjacent to the first side of the microfeature workpiece to form a conductive plug; and

a second conductive material (Fig 13C element 30; Fig 17B element 8; Figs 33 element 104) deposited in a second portion of the passage in contact with the conductive plug to at least generally fill the passage from the conductive plug to the second side of the microfeature workpiece.

Regarding claim 36: Hayasaka discloses the microfeature workpiece of claim 33, further comprising an insulative layer (Fig 13C, 17B element 14; Fig 14D element 31) deposited in the passage between the die (10/11) and the first and second conductive materials (Fig 13C elements 29/30; Fig 14D, element 15; Fig 17B elements 15/8).

Regarding claim 38: Hayasaka discloses the microfeature workpiece of claim 33, further comprising a bond-pad (Fig 14D, element 17) formed on the first side of the microfeature workpiece in contact with the conductive plug (Fig 14D, element 15).

Regarding claim 50: Hayasaka discloses the microfeature workpiece of claim 33, further comprising an insulative layer (Fig 13C, 17B element 14; Fig 14D element 31)deposited in the passage, wherein the second conductive material contacts the conductive plug and the insulative material (see Fig 13C, 17B).

Regarding claim 39: Hayasaka discloses a microelectronic device (examples in Fig 4, Fig 13C, 14D, and 17B) set comprising:

a first microelectronic device (Fig 4 element 1b) having:

a first die (Fig 4 element 2; Fig 13C element 11, Fig 14D element 11; Fig 17B element 11) with a first integrated circuit (integrated circuit within element 11 shown in Figure 9) and a first bond-pad (Fig 4 element 6; Fig 14D element 17) electrically coupled to the first integrated circuit, the first die further including a passage (Fig 13C element 13) extending completely through the first die and the first bond-pad (col 16 lines 42-45); and

a conductive interconnect (Fig 4 element 5) deposited in the passage, the conductive interconnect including a first conductive material (Fig 13C element 29; Fig 14D, element 15; Fig 17B element 15) deposited in a first portion of the passage to form a conductive plug, and a second conductive material (Fig 13C element 30; Fig 17B

element 8) deposited in a second portion of the passage in contact with the conductive plug to at least generally fill the passage; and

at least a second microelectronic device (Fig 4 element 1a) having a second die (Fig 4 element 2; Fig 13C element 11, Fig 14D element 11; Fig 17B element 10) with a second integrated circuit (integrated circuit within element 11 shown in Figure 9) and a second bond-pad (Fig 4 element 6; Fig 14D element 17) electrically coupled to the second integrated circuit, wherein the second bond-pad is electrically coupled to the conductive interconnect of the first microelectronic device (Fig 4; col 10 lines 30-34).

Regarding claim 40: Hayasaka discloses the microelectronic device set of claim 39 wherein the first microelectronic device (Fig 4 element 1b) is attached to the second microelectronic device (Fig 4 element 1a) in a stacked-die arrangement (see Figure 4).

Regarding claim 41: Hayasaka discloses the microelectronic device set of claim 39, further comprising a solder ball (Figure 4 element 8) disposed between the conductive interconnect (3) of the first microelectronic device (1a) and the second bond-pad (6) of the second microelectronic device (1a) to electrically couple the first bond-pad to the second bond-pad (col 10 lines 30-34).

Regarding claim 42: Hayasaka discloses the microelectronic device set of claim 39 wherein the passage (Fig 13C element 13) is a first passage, wherein the second microelectronic device (Fig 4 element 1a) further includes a second passage (Fig 13C element 13) extending through the second die (Fig 4 element 2; Fig 13C element 11, Fig 14D element 11; Fig 17B element 10) and the second bond-pad (Fig 4 element 6;

Fig 14D element 17), and wherein the second passage is completely filled with a third conductive material (Fig 4 element 5).

Regarding claim 43: Hayasaka discloses the microelectronic device set of claim 39 wherein the first microelectronic device (Fig 4 element 1b) further includes a redistribution layer (3) formed on the first die, the redistribution layer including a conductive line (multilayer interconnect; col 10 line 1) having a first end portion attached to the first bond-pad and a second end portion positioned outward of the first end portion, wherein the second end portion is configured to receive electrical signals and transmit the signals to at least the first integrated circuit of the first die and the second integrated circuit of the second die (col 10 lines 30-34).

Regarding claim 51: Hayasaka discloses the microelectronic device set of claim 39 wherein the first microelectronic device (Fig 4 element 1b) further includes an insulative layer (Fig 4 element 5, Fig 13C element 14, Fig 14D element 31, and Fig 17B element 14) deposited in the passage, and wherein the second conductive material contacts the conductive plug and the insulative layer (see Fig 17B).

Regarding claim 44: Hayasaka discloses a microelectronic device set (examples in Fig 4, Fig 13C, 14D, and 17B) comprising:

a first microelectronic device (Fig 4 element 1b) having:

a first die (Fig 4 element 2; Fig 13C element 11, Fig 14D element 11; Fig 17B element 11) with a first integrated circuit (integrated circuit within element 11 shown in

Figure 9) and a first bond-pad (Fig 4 element 6; Fig 14D element 17) electrically coupled to the first integrated circuit, the first die further including a passage aligned with the first bond-pad (shown in Fig 4 and Fig 14D); and

a conductive interconnect (Fig 4 element 5) deposited in the passage, the conductive interconnect including a first conductive material (Fig 13C element 29; Fig 14D, element 15; Fig 17B element 15) deposited in a first portion of the passage to form a conductive plug in contact with the bond-pad, and a second conductive material (Fig 13C element 30; Fig 17B element 8) deposited in a second portion of the passage in contact with the conductive plug to at least generally fill the passage; and

at least a second microelectronic device (Fig 4 element 1a) having a second die (Fig 4 element 2; Fig 13C element 11, Fig 14D element 11; Fig 17B element 10)with a second integrated circuit (integrated circuit within element 11 shown in Figure 9) and a second bond-pad (Fig 4 element 6; Fig 14D element 17) electrically coupled to the second integrated circuit, wherein the second bond-pad is electrically coupled to the first bond-pad of the first microelectronic device (Fig 4; col 10 lines 30-34).

Regarding claim 45: Hayasaka discloses the packaged microelectronic device of claim 44, further comprising an insulative layer (Fig 13C, 17B element 14; Fig 14D element 31) deposited in the passage (13) between the first die (Fig 4 element 2; Fig 13C element 11, Fig 14D element 11; Fig 17B element 11) and the first and second conductive materials (Fig 13C elements 29/30; Fig 14D, element 15; Fig 17B elements 15/8).

Regarding claim 52: Hayasaka discloses the microelectronic device set of claim 44 wherein the first microelectronic device (Fig 4 element 1b) further includes an insulative layer (Fig 4 element 5, Fig 13C element 14, Fig 14D element 31, and Fig 17B element 14) deposited in the passage, and wherein the second conductive material contacts the conductive plug and the insulative layer (see Fig 17B).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,809,421 to Hayasaka et al. (Hayasaka) in view of U.S. Pat. No. 7,045,015 to Renn et al. (Renn).

Regarding claim 2, Hayasaka discloses the method of claim 1, as above, and forming a conductive plug by depositing an electrically conductive material in the passage. Hayasaka lacks disclosing depositing an electrically conductive material by using a maskless mesoscale materials deposition process. Renn discloses using a maskless mesoscale materials deposition process to deposit an electrically conductive material (col 8 lines 24-26). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hayasaka to have the electrically conductive material deposited by a maskless mesoscale materials deposition process

as in Renn because the process can deposit fine features on low-temperature or high-temperature substrates (col 2 lines 22-25).

Claims 3 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,809,421 to Hayasaka et al. (Hayasaka) in view of U.S. Pub. No. 2004/0087441 to Hirakata et al. (Hirakata).

Regarding claims 3 and 34, Hayasaka discloses the method of claims 1 and 33 and 44 as above. Hayasaka lacks disclosing forming a conductive plug includes applying an electronic ink in the passage using an electronic printing process. Hirakata teaches forming a conductive plug includes applying an electronic ink (conductive paste; paragraph 102) in the passage using an electronic printing process (ink jetting; paragraph 102). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the conductive e plug by applying an electronic ink using an electronic printing process as in Hirkata because with electronic printing processes the plug only needs to be formed in the desired area therefore wasted material is reduced.

Claims 31 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,809,421 to Hayasaka et al. (Hayasaka) in view of U.S. Pat. No. 6,703,310 to Mashino et al. (Mashino) and U.S. Pub. No. 2004/0087441 to Hirakata et al. (Hirakata).

Regarding claims 31 and 46, Hayasaka discloses the method of claims 28 and 44 as above. Hayasaka fails to disclose wherein forming the passage extends through the bond-pad and wherin the first conductive material is in contact with an exposed surface of the bond pad.

Mashino teaches a method of forming a microelectronic device (Figures 1-8, element 215) further comprising forming a bond-pad (211) on the microelectronic workpiece, wherein the passage (212) extends through the bond-pad (Figure 4L) and the first conductive material is in contact with an exposed surface of the bond pad. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hayasaka to have the passage through the bond-pad as in Mashino in order to have the bond pad and plug be electrically connected through the passage.

Hayasaka and Mashino fail to disclose forming a conductive plug includes applying an electronic ink in the passage using an electronic printing process. Hirakata teaches forming a conductive plug includes applying an electronic ink (conductive paste; paragraph 102) in the passage using an electronic printing process (ink jetting; paragraph 102). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the conductive plug by applying an electronic ink using an electronic printing process as in Hirkata because with electronic printing processes the plug only needs to be formed in the desired area therefore wasted material is reduced.

Claims 4 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,809,421 to Hayasaka et al. (Hayasaka) in view of U.S. Pub. No. 2004/0087441 to Bock et al. (Bock).

Regarding claims 4 and 35, Hayasaka discloses the method of claims 1 and 33 as above. Hayasaka fails to disclose depositing an electrically conductive material in the passage using a nano-particle deposition process. Bock teaches using a nano-particle process to deposit a conductive material (abstract lines 15-20). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hayasaka to have the electrically conductive material deposited by a nano-particle process as in Bock because the process can deposit fine features.

Claims 6-8, 11 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,809,421 to Hayasaka et al. (Hayasaka) in view of U.S. Pat. No. 6,703,310 to Mashino et al. (Mashino).

Regarding claim 6, Hayasaka discloses the method of claim 1, further comprising forming a bond-pad (Fig 14D element 17) on the microelectronic workpiece and forming the passage (Fig 14D element 13). Hayasaka fails to disclose wherein forming the passage includes forming the passage through the bond-pad, and wherein forming a conductive plug in the passage includes depositing a conductive material to contact an exposed surface of the bond-pad.

Mashino teaches a method of forming a conductive interconnect in a microelectronic device (Figures 1-8, element 215) further comprising forming a bond-

pad (211) on the microelectronic workpiece, wherein forming the passage (212) includes forming the passage through the bond-pad (Figure 4L), and wherein forming a conductive plug in the passage includes depositing a conductive material to contact an exposed surface of the bond-pad (col 6 lines 65-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hayasaka to have the passage through the bond-pad as in Mashino in order to have the bond pad and plug be electrically connected through the passage.

Regarding claim 7, Hayasaka discloses the method of claim 1. Hayasaka fails to discloses where forming the passage includes laser drilling the passage through the die. Mashino teaches where forming the passage includes laser drilling (Figure 4L, col 9 line 37- col 10 line 4) the passage through the die. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hayasaka to form the passage using laser drilling to cleanly form the passage.

Regarding claim 8, Hayasaka discloses the method of claim 1 where providing a microfeature workpiece includes providing a die having an integrated circuit (integrated circuit within element 11 shown in Figure 9) and a bond-pad (Fig 14D element 17) electrically coupled to the integrated circuit.

Hayasaka fails to disclose wherein forming the passage (212) includes laser drilling (Figure 4L, col 9 line 37- col 10 line 4) the passage through the die and the bond pad (col 6 lines 58-59).

Mashino teaches where providing a microfeature workpiece includes providing a die having an integrated circuit (202) and a bond-pad (211) electrically coupled to the

integrated circuit (col 6 lines 50-52), and wherein forming the passage (212) includes laser drilling (Figure 4L, col 9 line 37- col 10 line 4) the passage through the die and the bond pad (col 6 lines 58-59). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hayasaka to form the passage using laser drilling to cleanly form the passage.

Regarding claim 11, Hayasaka discloses the method of claim 1 where depositing conductive material in the passage to at least generally fill the passage (13). Hayasaka fails to discloses biasing the conductive plug at an electrical potential.

Mashino teaches wherein depositing conductive material in the passage to at least generally fill the passage includes biasing the conductive plug at an electrical potential (power feed layer 205a, can provide an electrical potential). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hayasaka to biasing the conductive plug at an electrical potential as in Mashino in order to allow for device operation.

Regarding claim 30, Hayasaka discloses the method of claim 28, including the passage (Fig 14D element 13) and bond-pad (Fig 14D element 17) and further comprising an insulative layer (Fig 13C, 17B element 14; Fig 14D element 31) deposited in the passage between the die and the first and second conductive materials. Hayasaka fails to disclose wherein forming the passage extends through the bond-pad.

Mashino teaches a method of forming a microelectronic device (Figures 1-8, element 215) further comprising forming a bond-pad (211) on the microelectronic

workpiece, wherein the passage (212) extends through the bond-pad (Figure 4L). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hayasaka to have the passage through the bond-pad as in Mashino in order to have the bond pad and plug be electrically connected through the passage.

Claims 32 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,809,421 to Hayasaka et al. (Hayasaka) in view of U.S. Pat. No. 6,703,310 to Mashino et al. (Mashino) and U.S. Pub. No. 2004/0087441 to Bock et al. (Bock).

Regarding claims 32 and 47, Hayasaka discloses the method of claims 28 and 44 as above. Hayasaka fails to disclose wherein forming the passage extends through the bond-pad and wherin the first conductive material is in contact with an exposed surface of the bond pad.

Mashino teaches a method of forming a microelectronic device (Figures 1-8, element 215) further comprising forming a bond-pad (211) on the microelectronic workpiece, wherein the passage (212) extends through the bond-pad (Figure 4L) and the first conductive material is in contact with an exposed surface of the bond pad. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hayasaka to have the passage through the bond-pad as in Mashino in order to have the bond pad and plug be electrically connected through the passage.

Hayasaka and Mashino fail to disclose depositing an electrically conductive material using a nano-particle deposition process. Bock teaches using a nano-particle process to deposit a conductive material (abstract lines 15-20). It would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Hayasaka to have the electrically conductive material deposited by a nano-particle process as in Bock because the process can deposit fine features.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,809,421 to Hayasaka et al. (Hayasaka) in view of U.S. Pat. No. 6,828,223 to Chuang.

Regarding claim 5, Hayasaka discloses the method of claim 1 where forming a conductive plug includes depositing a metal into the passage (col 12 lines 56-57). Hayasaka fails to disclose the metal as silver. Chuang teaches using silver as a conductive plug (col 1 lines 11-21). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Hayasaka to have the metal be silver as in Chuang because silver has low-resistivity and is a good electrical conductor.

Response to Arguments

Applicant's arguments with respect to claims 1-11, 28-36, 38-52 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Colleen A. Matthews whose telephone number is 571-272-1667. The examiner can normally be reached on Monday - Friday 8AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CAM
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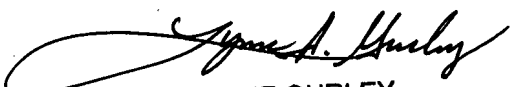

LYNNE GURLEY
SUPERVISORY PATENT EXAMINER
AU 2811, TC 2800